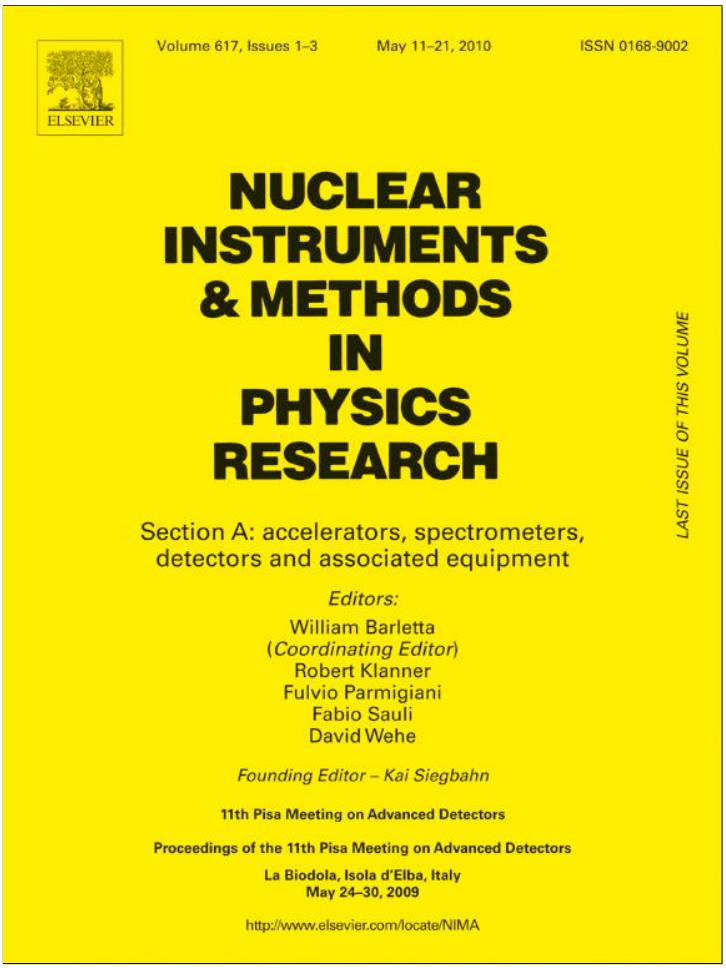

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3D design activities at Fermilab—Opportunities for physics

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ABSTRACT

Fermilab began exploring the technologies for vertically integrated circuits (also commonly known as 3D circuits) in 2006. These technologies include through silicon vias (TSV), circuit thinning, and bonding techniques to replace conventional bump bonds. Since then, the interest within the High Energy Physics community has grown considerably. This paper will present an overview of the activities at Fermilab over the last 3 years which have helped spark this interest.

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1. Bonding technologies

Bonding along with precision alignment are critical components of 3D integration. Die to wafer bonding results in the highest circuit yield, while wafer to wafer bonding results in the lowest cost per mated circuit. Fermilab has worked with multiple vendors with different bonding technologies over the last 3 years.

1.1. Bonding techniques to replace bump bonds

A study which compared soldering with copper tin (CuSn) pillars shown in Fig. 1 to conventional lead tin (PbSn) solder bumps was completed with RTI International [1]. The CuSn pillars and PbSn bumps were about 10 μm high. It was found that CuSn bonding produced higher yields and stronger bonds than the PbSn bonding at a 20 μm pitch. The cost of CuSn bonding can be relatively low. If post-bond thinning is necessary, a significant percentage of the chip surface area should be covered with CuSn to avoid circuit warping and die shear. This can unfortunately lead to a relatively high material budget.

Another approach for bump bond replacement was tested by using the Direct Bond Interconnect (DBI) technology from Ziptronix to bond 25 sensors to a readout chip wafer as shown in Fig. 2. A very small percentage of the mated surface area was covered with metal contacts. After bonding the sensor chips to the readout circuit wafer, the sensors were thinned to 100 μm. No warping or chip separation occurred and a reasonable bond yield was obtained. Future work will thin chips to 25 μm or less after DBI bonding. The DBI process begins with very small metal contacts imbedded in a smooth oxide surface. When the two oxide surfaces are brought together, an oxide bond is immediately formed. After the oxide bond reaches sufficient strength, the devices are heated and the metal contacts expand to form compression bonds. Minimal mass is needed for the bonding, thus making this an excellent choice for applications such as the International Linear Collider vertex detector.

1.2. Bonding techniques for 3D chip fabrication

Fermilab began its 3D circuit design activities by using the MIT Lincoln Laboratory 180 nm SOI process with oxide bonding between the wafers to build 3 tier circuits. The MIT process is a "via last" process which means that vias between bonded wafers are added after the standard wafer fabrication is completed.

More recent design work at Fermilab has focused on the Tezzaron process using CMOS wafers with a copper to copper wafer bond interface. Tezzaron uses a "via first" process where TSVs are added to the wafers at the foundry just after the fabrication of the transistors. Wafers with the TSV are fabricated in the Chartered 130 nm process. Although as many as five stacked layers have been demonstrated by Tezzaron, our designs currently only use two layers.

2. Consortium for 3D circuit design

Based on the success of the first 3D design at Fermilab and the opportunity to establish 3D multi-project runs specifically for HEP, a number of institutions have come together and formed a consortium for 3D circuit design. The international consortium with 15 members from 5 different countries is completing work on its first 3D multi-project run with Tezzaron. There are over 25

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designs of complete circuits and test structures. The circuit designs are aimed at ATLAS pixels, CMS silicon strips, ILC pixels, B factory pixels, and X-ray imaging. The test circuits are intended to study radiation tolerance, cryogenic operation, bond and via reliability, and SEU tolerance. To reduce costs, only a single set of masks are used for both the top and bottom layers of the 3D circuit. Designs up to $5.5 \times 6.3\,mm^2$ have been accommodated in the $26 \times 30\,mm^2$ frame.

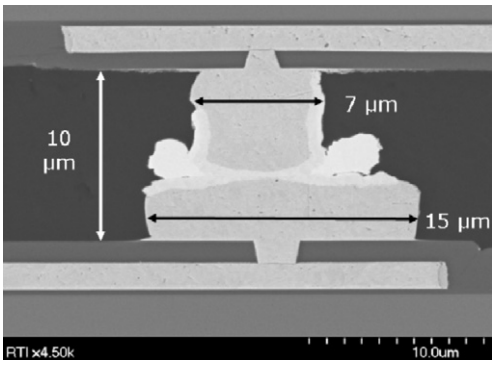

Fig. 1. Cross-section of CuSn bond.

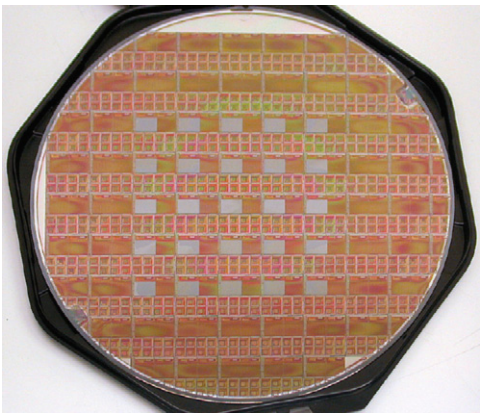

Fig. 2. 25 sensors mounted with DBI.

3. Vertically integrated circuits by Fermilab

At the present time, Fermilab has completed design of five 3D integrated circuits. Two of the circuits were completed in the MIT LL SOI process. These circuits were full function demonstrator chips for an ILC pixel detector. The first chip, VIP1, included many features: 20 μm pixels in a 4 K array, read out between ILC bunch trains, high speed data sparsification, analog output for improved resolution, and 5 bit digital stamping for 30 μs resolution. Fig. 3 shows how a single pixel schematic is divided into 3 tiers [2]. Although the VIP1 was found to be functional the yield was very low. Thus another version of the chip (VIP2a) was submitted to MIT LL with numerous changes including: improved power distribution, wider traces, redundant vias, and some circuit changes. VIP2a is still in fabrication.

After VIP2a, the focus at Fermilab shifted toward using a commercial CMOS process for higher yield and radiation tolerance. Thus the next three circuits were designed in the Chartered 130 nm CMOS process using the Tezzaron 3D approach. The first circuit was a redesign of the VIP2a from a 3 tier circuit to a 2 tier circuit. The new circuit called VIP2b is a larger array (192×192) with 8 bits of time stamping for better time resolution (3.9 μs), and a larger pixel size of 24 μm to accommodate the larger time stamp.

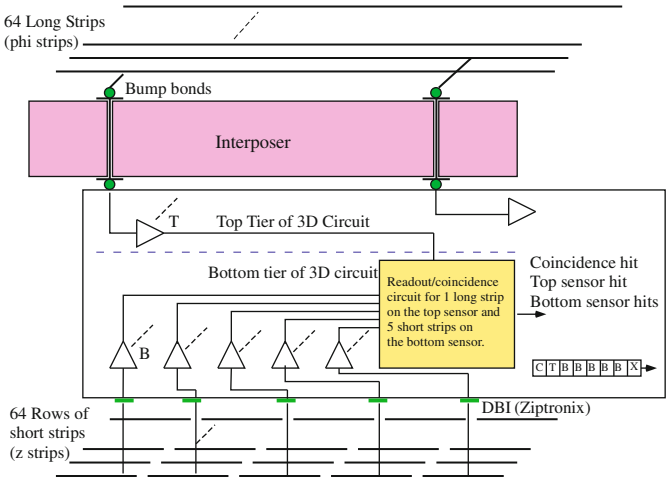

Fig. 4. Block diagram of a portion of the VICTR chip and the top and bottom sensors.

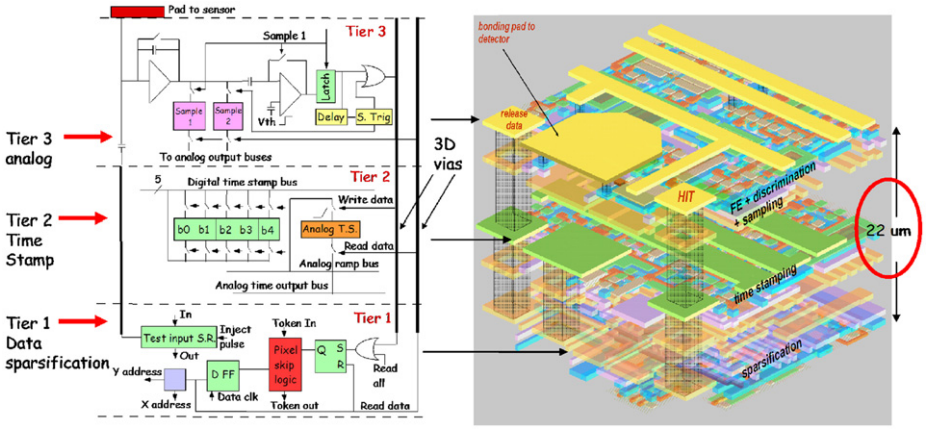

Fig. 3. 3D schematic and layout for 1 pixel VIP1 pixel cell.

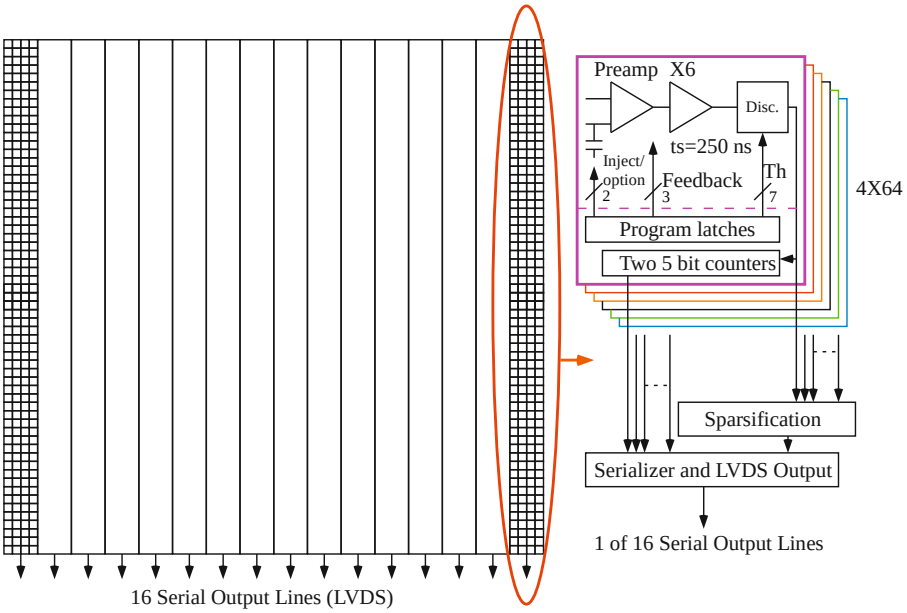

Fig. 5. Block diagram of VIPIC.

The next 3D chip represents a first step toward developing a Level 1 track trigger for Super CMS using sensor pairs. To reduce track hit data, the track trigger must (1) identity hits associated with pt above 2 GeV for data transfer, (2) rapidly identify tracks with pt above 15–25 GeV, and (3) provide good *Z* vertex resolution of about 1 mm for tracks above 2 GeV [3]. To identify hits with pt above 2 GeV, two 80 μm pitch sensor barrels, one with long silicon strips and the other with short strips are separated by a 1 mm interposer as shown in Fig. 4. Stiff tracks have nearly vertical tracks between the sensors. A hit in a long strip gives phi information and a hit on the shorter strips gives *Z* information. The 3D chip called VICTR (Vertically Integrated CMS TRacker) collects hits from both sensors and finds hit pairs with pt >2 GeV by means of a coincidence circuit. In the final circuit, the simple coincidence circuit will take into account neighbor strips. The chip is only 24 μm thick and by means of top and bottom connections is mounted between the interposer and bottom sensors. A simplified block diagram of the top and bottom sensors and a portion of the VICTR chip are shown in Fig. 4.

The last chip was designed for X-ray photon correlation spectroscopy to study the dynamics of equilibrium and non-equilibrium processes. The chip called VIPIC (Vertically Integrated Photon Imaging Chip) is a 64×64 array of 80 μm pixels. The array has a sparsified binary data output with a read out time of 10 μs for occupancies of $\sim$100 photons/cm^2/s. It operates in a dead timeless, trigger less mode and is optimized for 8 keV photons. The chip is 5.5×6.3 mm^2 and features two 5 bit counters for recording of multiple hits per time slice, thus also providing imaging information. The pixel address read out time is constant regardless of hit location due to use of a binary tree hit finder. The pixel array is read out on 16 parallel high speed LVDS output lines as shown in Fig. 5. The design is adaptable to 4 side buttable X-ray detectors arrays.

4. Conclusion

Fermilab has acquired experience with several 3D technologies, two of which have been used to successfully replace conventional bump bonds. Two other bonding processes have been used for fabrication of 3D integrated circuits. Based on the early design efforts at Fermilab, a large consortium of institutions has come together to develop 3D integrated circuits for physics applications. The five circuits designed by Fermilab suggest the wide range of applications that are possible with 3D integration.

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